Electromagnetic/Circuit Co-optimization of Lumped Component and Physical Layout Parameters using Generalized Layout Components

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Abstract — **This paper describes the concept of a generalized parametric layout component which enables to simultaneously optimize the physical layout variations together with lumped passive and active component parameters. This is realized by a seamless integration of a electromagnetic simulator within a circuit simulation and optimization tool. The electromagnetic S-parameter model is generated dynamically for each set of layout component parameters, as selected by the optimizer. An electromagnetic model database keeps track of the generated S-parameter models for later reuse. This concept is illustrated in the design of a RF board low noise amplifier circuit.**

I. INTRODUCTION

Over the past decade, planar electromagnetic simulators [1-4] have been extensively used for the physical verification of layout interconnects in RF board and microwave circuit applications. During a circuit simulation, the physical effects of the interconnect are represented by a so-called 'layout component'. The footprint of such a component consists of the interconnect, via and ground plane metal and the electrical model is linked to a S-parameter file as generated by the electromagnetic (EM) simulator. This design flow has mainly been a manual and static process. The S-parameter model needs to be calculated up-front and is manually linked to the layout component. The latter approach has some important drawbacks. To be practical, the number of ports is limited, the back annotation of the electromagnetic simulation results and the interconnection with other components is tedious and error prone and the verification and optimization of layout variations is a manual and engineer-time consuming iterative process.

In [5], direct EM optimizations were presented for the first time, allowing to reach the design specifications with full EM accuracy, by automatically adjusting physical layout variations in the design. In this approach the optimizer directly drives the EM engine. An integrated EM optimization with nonlinear Harmonic Balance simulation is presented in [6], enabling to fully optimize the physical layout in conjunction with non-linear circuit performance.

Building upon these concepts, we have integrated a commercially available circuit simulator between the circuit optimizer and our EM engine and generalized the concept of a parametric layout component. This approach provides an automated and user friendly way to integrate EM simulations in a circuit design environment preserving the full flexibility to combine time domain (Transient) or frequency domain circuit analysis (DC, AC, Harmonic Balance, Envelope,...) with EM generated models. During the circuit optimization process, both lumped component and physical layout parameters can vary simultaneously in order to realize the specified goals. The EM model generation process is seamlessly integrated as part of the circuit simulation. The circuit simulation engine will, when encountering a 'generalized layout component', check its EM model database for the availability of the required model. When missing, the EM engine will be invoked to generate the model which is afterwards stored as part of the database.

II. GENERALIZED LAYOUT COMPONENTS

The generalized layout components are defined and parameterized, starting from an existing layout built with primitive artwork shapes and/or existing layout components. Two types of parameters are added to generalize the component definition: model control and layout parameters. The model control parameters determine the setup of the electromagnetic simulation during the S-parameter model generation. They specify the mesh settings and the frequency range for the S-parameter models and can take only discrete values. Layout parameters are captured by either defining a layout perturbation for the primitive artwork shapes associated with the parameter variation or by using one or more of the existing layout component parameters. The layout parameter values can vary in a continuous way.

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The schematic symbol created for the layout component is layout look-alike in the sense that the actual layout artwork is used in combination with an appropriate scaling factor to draw the symbol. The layout look-alike symbol automatically maps the schematic pins of the symbol with the physical locations of the layout ports, facilitating the interconnection with lumped passive and active components in the schematic design.

Figure 1 shows the schematic design of a low noise amplifier circuit. The active element is a double emitter bipolar junction transistor (Agilent AT41411 with SOT143 package) for which a Gummel-Poon NPN model is available. Figure 2 shows the RF board layout footprint for this amplifier design.

In order to include the RF board layout effects in the circuit simulation, a generalized layout component was created. The layout parameterization is illustrated by defining one layout parameter 'Pvia', allowing to vary the position of one of the grounding vias along the arrow shown in Figure 2. The complete schematic of the LNA design, including the generalized layout component for the RF board layout footprint and the lumped components, is shown in Figure 3. The size of the layout look-alike symbol is chosen such that the lumped components fit between each pair of schematic pins.

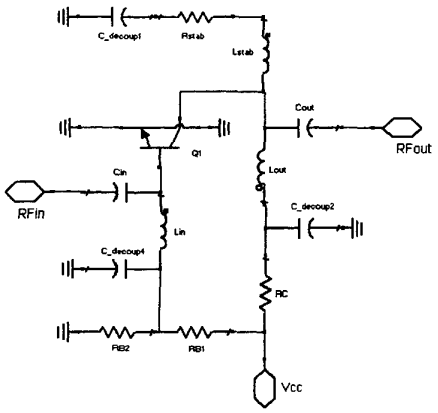

Figure 1. Schematic design for the low noise amplifier

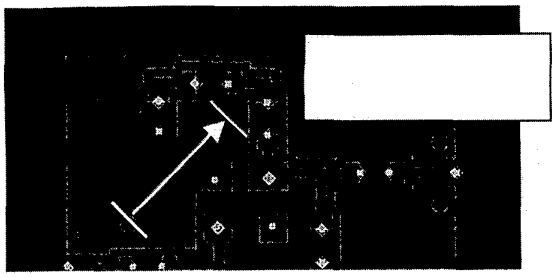

Figure 2. RF board layout footprint for the low noise amplifier design.

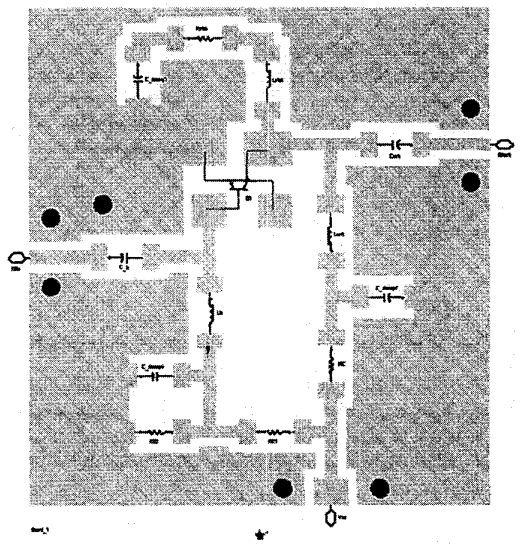

Figure 3. Schematic design for the low noise amplifier including the generalized RF board layout component.

III. Electromagnetic Model Database

The diagram in Figure 4 depicts the building blocks and their dynamic links during an EM/Circuit co-optimization process. The layout components are parsed from the input netlist. The model control and layout parameters are set by the user or automatically selected by the optimizer and passed through the circuit simulator to the dynamically linked electromagnetic engine. A S-parameter model for the layout component is generated during the circuit

optimization if the component is being simulated for the first time.

An electromagnetic model database between the circuit simulator and the EM engine keeps track of the generated S-parameter model samples. Database model interpolation is checked upon for varying layout parameters. As gradient based circuit optimizers cannot cope with numerical noise in the generated S-parameters, a linear interpolation scheme is implemented in the EM model database. This avoids the generation of S-parameter models for very small layout variations. The smallest allowable variation for the layout parameters is derived from the selected model control parameter values.

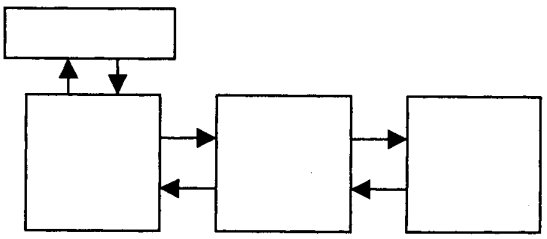

Figure 4. Block diagram of EM/Circuit co-optimization flow.

The interpolation scheme is dynamic, in the sense that it automatically determines the minimum number of additional samples needed to obtain an interpolated result for the requested parameter values. This minimizes the number of time-consuming EM simulations during the circuit optimization.

IV. NUMERICAL RESULTS

The amplifier gain for the LNA design was simulated using the Advanced Design System (ADS) software from Agilent Technologies. The numerical results for the original schematic design (Figure 1) are shown in Figure 6. The amplifier gain reaches a peak of 19 dB at about 0.5 GHz. Next, the RF board layout effects were included in the design (Figure 3) using the generalized layout component and an EM/circuit co-simulation was run. The Momentum electromagnetic simulator was used to obtain the S-parameter model for the RF board layout. Including the board layout parasitics in the simulation has the effect of lowering the amplifier gain more than 1dB as can be seen in Figure 6.

In order to optimize the performance of the amplifier response, an EM/circuit co-optimization was run. Figure 5 shows the optimization setup and the biasing for the LNA design in ADS. Two design parameters were setup to vary during the optimization process: the lumped capacitance value of input capacitor 'Cin' and the position of the grounding via set by the value of the physical layout parameter 'Pvia'. The optimization goal was specified to maximize the amplifier gain in the frequency range from 0.4 GHz to 0.6 GHz. The starting values for the parameters were: Pvia=20mil and Cin=12pF. The gradient based optimization stopped after 13 iterations due to zero gradients with optimal parameter values: Pvia=89.73mil and Cin=120pF. Note that for the optimal design parameters, the grounding via is positioned closest to the emitter contact of the bipolar transistor.

The amplifier gain for the optimal design parameters is plotted in Figure 6. The optimized amplifier gain now reaches a peak of 19.5 dB at 0.5 GHz, which is an improvement of almost 2 dB. The complete optimization run was finished in 54min 33sec (HP Kayak XA, Pentium II, 330 MHz). A total of 11 electromagnetic samples were required to characterize the RF board layout, each taking up about 2m28s of the overall simulation time.

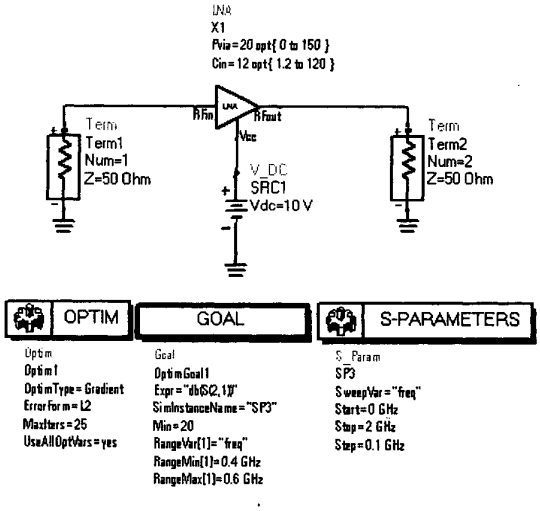

Figure 5. Optimization setup for the LNA design.

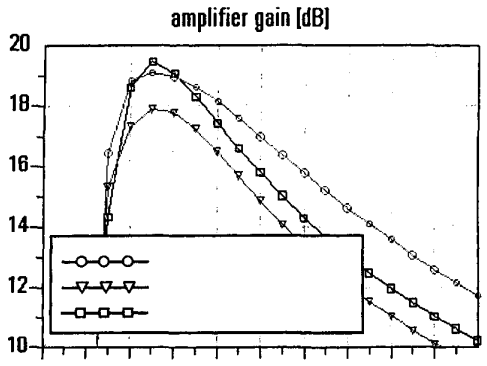

Figure 6. Amplifier gain for original and optimized design.

IV Conclusion

We introduced the concept of a generalized layout component in a schematic design enviroment. The main contribution of this concept is that it enables EM/Circuit co-optimization by simultaneously varying lumped component and physical layout design parameters in a user friendly way with full flexibility to combine time domain (Transient) or frequency domain circuit analysis (DC, AC, Harmonic Balance, Envelope,...) with EM generated models. Layout components streamline the virtual design and verification process of analog RF and Microwave circuit performance including the physical layout effects.

References

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